REMARKS

Claims 1-15 are pending. No new matter has been added.

Disclaimers Relating to Claim Interpretation and Prosecution History Estoppel

Claims 1 and 10 have been amended notwithstanding the belief that these claims were allowable. Except as specifically admitted below, no claim elements have been narrowed. Rather, cosmetic amendments have been made to the claims and to broaden them in view of the cited art. The amendments to claims 1 and 10 were not necessary for patentability.

Any reference herein to "the invention" is intended to refer to the specific claim or claims being addressed herein. The claims of this Application are intended to stand on their own and are not to be read in light of the prosecution history of any related or unrelated patent or patent application. Furthermore, no arguments in any prosecution history relate to any claim in this Application, except for arguments specifically directed to the claim.

Priority Claim

The Application claims priority as a CIP. The priority claim was reported in the Filing Receipt. However, the Office Action does not indicate that the Examiner acknowledged the priority claim. It is therefore requested that the next Office Action include an acknowledgement of the priority claim.

Drawings

Formal drawings are being transmitted separately, via mail.

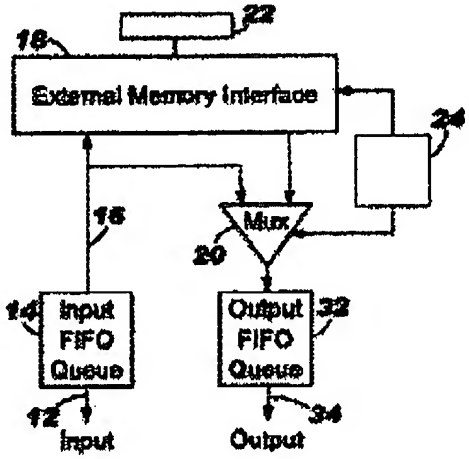
Specification

The Examiner objected to the specification because of a number of informalities. This objection is respectfully traversed. The informalities identified by the Examiner have been addressed.

Claim Rejections - 35 USC § 102

The Examiner rejected claims 1-11 under 35 USC § 102(e) as anticipated by Bass et al (USP 6,557,053). This rejection is respectfully traversed.

Bass is directed to a queue manager for a buffer. Bass discloses an input FIFO 14,[1] an output FIFO 32, an external memory 22, a multiplexer 20 and control logic 24:



In Bass, data leaving the input FIFO 14 goes to both the external memory 22 and the mux 20. Furthermore the mux can select data from either the memory 22 or the input FIFO 14. This is controlled by the control logic 24. The input FIFO and output FIFO are smaller and faster than the external memory. Bass discloses and teaches that the control logic 24 is used to maximize utilization of the input FIFO and the output FIFO. The control logic 24 directs data into the output FIFO so long as the input FIFO and output FIFO "are full or at least have a predetermined percentage capacity full."[2] "Thus, as long as the amount of input data 12 being read from an external source does not

[1] The arrow on the data input 12 appears to be pointing the wrong way.
[2] Bass 2:21-24.

exceed a preselected capacity of the input FIFO buffer 14 and output FIFO buffer 32, the data is passed from the input FIFO buffer 14 directly to the output FIFO buffer32."[3]

The invention of claim 1 is a caching system which includes a tail FIFO, a memory, a head FIFO, a multiplexer and a controller. The controller is "operable to transfer one or more blocks of the incoming data having a selected block size from the tail FIFO to the memory and from the memory to the head FIFO, wherein the selected block size provides a selected memory transfer efficiency level." The "memory transfer efficiency level" relates to the efficiency of the memory's data transfers.

Bass has no disclosure, teaching or suggestion of selecting a block size for transferring data between a FIFO and a memory to provide a selected memory transfer efficiency level. Notably, in rejecting claim 1, the Examiner did not address this limitation. Bass is directed to utilization of the FIFOs at a maximum or predetermined level. This is certainly different from selecting a block size which provides a selected memory transfer efficiency level as recited in claim 1. Thus, claim 1 is not anticipated or rendered obvious by Bass.

The invention of claim 10 is a method for implementing a caching system. Claim 10 recites the step of "selecting an efficiency level for operating a memory interface." Claim 10 further recites the step of "determining a selected block size to support the efficiency level."

Bass has no disclosure, teaching or suggestion that either of these two steps of claim 10 be performed. In rejecting claim 10, the Examiner appears to have confused Bass' control of FIFO capacity utilization with claim 10's control of memory transfers to achieve a selected efficiency level. Thus, claim 10 is not anticipated or rendered obvious by Bass.

In sum, the rejection of claims 1-12 as anticipated by Bass should be withdrawn.

[3] Bass 2:32-36.

Conclusion

It is submitted, however, that the independent and dependant claims include other significant and substantial recitations which are not disclosed in the cited references. Thus, the claims are also patentable for additional reasons. However, for economy the additional grounds for patentability are not set forth here.

In view of all of the above, it is respectfully submitted that the present application is now in condition for allowance. Reconsideration and reexamination are respectfully requested and allowance at an early date is solicited.

The Examiner is invited to call the undersigned attorney to answer any questions or to discuss steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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